Carbon Memory Assessment


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Outline: Carbon Memory Assessment

- Basic Facts about Carbon
  - Carbon Allotropes
  - Manipulating the Bond Structure of Carbon
  - Sustainable Current Density in Carbon Structures
  - Break-junctions and Plumbing in Carbon Structures
- What Is Not Considered as Carbon-based Memory
- Carbon-based Resistive Memory Phase Diagram
- First Current Pulse Challenge with Conductive Carbon
- Forming Challenge in Insulating Carbon
- Scaling of Carbon Memory
- Architectural Challenges for Resistive (Carbon) Memories
- Current State-Of-The Art For Carbon Memory Technology
- Selected Literature
Basic Facts about Carbon

- Carbon materials can have very different mass densities:
  - 4 mgcm\(^{-3}\) for nanotube-based aerogels
  - 0.2 - 1 gcm\(^{-3}\) for porous carbon
  - 2.2 gcm\(^{-3}\) for graphite
  - 3.5 gcm\(^{-3}\) for diamond

- The electronic properties range from metallic to semiconducting to insulating,

- The mechanical behavior cover everything, from soft to very hard

- Graphite is the most stable form and all other forms, especially sp\(^3\)-based bonds in diamond and ta-C favor the relaxed sp\(^2\)-bond
The Well-known Carbon Allotropes

Graphenic Carbon

Fullerens

Diamond

Graphene

Single-walled CNT

Multi-walled CNT
The Lesser-known Carbon Allotropes: a-C:H

Yellow balls represent one-fold carbon atoms, red balls are two-fold (sp1) atoms, white balls are three-fold (sp2) atoms, cyan ones are four-fold (sp3) atoms, and blue ones are hydrogen atoms.
The Lesser-known Carbon Allotropes: a-C:H

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Temperature stability: up to 450°C

tetrahedral amorphous carbon (ta-C) is produced by filtered cathodic vacuum arc (FCVA), mass-selected ion beam (MSIB), magnetron sputtering or laser ablation: temperature stable up to 900 °C
The **Lesser-known** Carbon Allotropes: ta-C

- ta-C with high density with high stress
- stress can induce a transformation from sp2 – to sp3
The Lesser-known Carbon Allotropes:
low mass density porous carbon, foam, ribbons….

- can be formed from carbides (TiC, SiC), pyrolysis of hydrocarbons, or spin-on deposition of carbon nanoparticles, fullerenes or nanotube solution,
Manipulating the Bond Structure of Carbon

- By stress relaxation, e-beams, electrical current, laser pulses, x-rays or temperature.
- Graphitization usually happens at above 2500 K,
- Small current can heal defects in nanotubes and graphene and even lead to the transformation of amorphous carbon into sp2-type carbon
- The power per volume is given by $j^2 \cdot \rho$, (current density $j$ and the specific resistivity $\rho$)
- 100 nA focused on a filament with 1 nm$^2$ cross-section, gives 10 MA/cm$^2$ !
- Delivered power density is MW/cm$^3$ to GW/cm$^3$
Manipulating Bonds by Laser Pulse

- Short laser pulse induces disorder (D-band)
- D-band overlaps with $sp^3$-peak at 1332 cm$^{-1}$
- Diamond cubic phase observed by e-beam diffraction

$\Rightarrow$ Disordered, quenched state by short energy pulse

Manipulating Bonds by Laser Pulse

- An increase of the average crystalline size of graphitic clusters occurs upon radiation performed at fluences of 300 and 400 mJ/cm².
- At higher energy density the material undergoes complete amorphization.
- Graphitization or, conversely amorphization of glassy carbon surface layers can be achieved by a proper choice of the laser irradiation conditions.

- Carbon behaves like a phase change material

Manipulating Bonds by Current

Increase of current

- By driving current thru the amorphous carbon (with high resistance), carbon is transformed into aligned sp2-bonded structures with low resistance.
- A short current pulse can transform the crystallized carbon again into an amorphous structure.

TEM image by courtesy of J. Huang et al., Nano Letters 2006 Vol. 6, No. 8 pp. 1699-1705
"In the **broken area**, nanotubes existed only on the surface and TEM & Raman show that the CNT structures were **completely changed** into other structures such as a graphite sheet or nanohorn, or a large diameter SWCNT other graphitic structures"
Sustainable Current Density in Carbon Structures

- **Sustainable current** density is as high as 400 MA/cm² in graphitic carbon or even up to 1GA/cm² in SWCNT.

- In **porous carbon** structures, the observed sustainable current densities are much lower and depend on the mass density of the carbon material.

- In **porous carbon** structures the current carrying parts have also high current densities, but averaging over the whole volume makes it drop.

- **Current pulse duration** in carbon needs to be as short as possible because otherwise surrounding material is destroyed and metallic electrodes molten.
Sustainable **Current Density** in MWCNT

- Prior to complete failure SiN dissociates at ~ 2173 K
  - hot carbon destroys other materials
- CNT fails at ~200 MA/cm² at ~3200 K
- Current pulses needs to be **as short as possible**

Sustainable Current Density in MWCNT

Critical current density of 350 MA/cm² observed

Appropriate cell diameter ~ 6 nm for I < 100 µA

Use spacer, cladding or self-assembled nano-pores

Sustainable **Current Density** in Electrodes

- A CNT in contact with a Au electrode
- At 1.5 V and 27μA the Au electrode melts and fills the CNT
- High current density not suitable for metallic electrodes
- Keep current pulses as short as possible

Break-junctions and Plumbing in Carbon Structures

- **Break junctions** can be created in carbon structures operated in **open systems** (like in a TEM, vacuum probe station, even in air) if the critical current density is reached.

- **On/Off switching** is observed in **break junctions** once a critical **electric fields** is achieved.

- This can be explained by **trapping of hydrocarbon gas** between the junction and subsequent pyrolysis in a bad vacuum (10^-7 mbar equals ~ 3⋅10^9 molecules/cm³).

- **Break junctions** can also be **created in porous carbon** that is encapsulated.

- Carbon structures separated by a short gap can be **plumbed** together by the application of an electric field. **Joule heating** from the **field emission current** will cause **atom diffusion** and **rearrangement of carbon**. Typical currents: 0.5 µA - 10 µA
**Break-junctions and Plumbing in Graphenic C**


Hydrocarbon Contamination in 10⁻⁷ mbar Vacuum

- Even in vacuum of 10⁻⁷ mbar, 3·10⁹ molecules/cm³ are present
- E-beam in SEM deposits this as carbon contamination on the sample
- The hydrocarbons can also be trapped by an electric field

Break-junctions and Plumbing in Graphenic C

- Trapping of hydrocarbons debris in a CNT-switch upon the application of an electric field
- Likely to be the main reason for on/off switching in open systems (TEM, vacuum probe station)

Break-junctions and Plumbing in SW-CNTs

Break-junctions and Plumbing in CNTs

When 1.0 V is applied between the MWNTs, the current increases to 15.6 μA and tips A and B coalesce at portions of the outermost wall layers.

Koji Asaka, Motoyuki Karita, Yahachi Saito, Joining of multiwall carbon nanotubes for the end-contact configuration by applying electric current, Materials Letters 65,1832–1834, (2011)
Break-junctions and Plumbing in CNTs

Atsuko Nagataki, Takazumi Kawai, Yoshiyuki Miyamoto, Osamu Suekane, Yoshikazu Nakayama, Controlling Atomic Joints between Carbon Nanotubes by Electric Current, PRL 102, 176808, (2009)
Break-junctions and Plumbing in Graphene

"Under such high activation energy due to high current heating, the attaching edges of two opposite GSs undergo atoms’ activation, diffusion and reconstructing to rearrange the carbon networks, such as hexagonal rings, pentagon–heptagon pairs, for seamless joining."

What Is Not Considered as Carbon-based Memory

- **diffusing metal ions** into insulating phases of carbon to form a resistive memory effect based on **metal filament creation and annihilation** [36, 37, 38, 49]
- **metal diffusion occurs** in almost all situations (like in ref. [37, 49]) where the capacitance discharge current from the first forming event is done by dc-voltage sweeps on samples with **no on-chip current limiter**, like on-chip resistors or transistors
- **SMU can neither limit** the capacitance discharge **current** nor a dc-current on a time scale shorter than ~30 µs
- Also not considered: **electronic memory effects** in insulating forms of carbon films. The **injected charge carriers** **modulate the tunnel barriers**, but this is a volatile effect.
Carbon-based Resistive Memory Phase Diagram

- two different mechanisms
  - low mass density: break-junction by local evaporation of carbon and plumbing by field emission
  - high mass density: conversion of a-C ↔ sp²-bonds
Field emission currents lead to rearrangement of the C-atoms and finally bridge the gap.

- $sp^2$-bonds bridge a nano-gap in porous carbon (on-state).
- The $sp^2$-bridge is deconstructed by a current pulse (~10 µA).

Inherently **scalable to atomic bonds**
Amorphous Carbon to $sp^2$-Bonds Conversion

- $sp^2$ to $sp^3$ conversion of disordered graphitic carbon (phase change of carbon)
- Inherently scalable to atomic bonds (no phases of different materials)
First Current Pulse Challenge with Conductive Carbon

- **First (!) current pulse** needs to destroy all conducting paths.
- The required current density (400 MA/cm²) is too high for high mass density graphenic carbon.
- Porous carbon might be accessible with ~10 MA/cm².
Forming Challenge with Insulating Carbon

- Capacitance discharge currents ($C\frac{dV}{dt}$) define $R_{on}$
- On-chip current limiter are needed (transistors)
- Forming voltage should be as low as possible (tunable by C-thickness)

My experience: cell $R_{\text{ON}}$ is defined by first (forming) $C \cdot dV/dt$

That's the reason why most ReRAM data have the same low $R_{\text{ON}}$, ($\sim 20$ kOhm) independent of the used material or stack

$I_{\text{cap}}$ reduction techniques include on-chip current limiter and high temperature forming

- Typical pad and probe tip have $C > 1$ pF
- Speed is within rise time of the scopes
- Relevant capacitance is within a sphere of $r = t \cdot v_{\text{prop}} < 100 \text{ps} \cdot v_{\text{prop}}$ (Wahlgren – horizon picture)
Scaling of Carbon Memory

- Scaling of carbon memory can go down to individual atomic bonds
- Open question are how much voltage and current is needed to create, maintain or destroy the atomic bonds
- Reported currents are around and below 10 µA

Scaling of Carbon Memory: structural examples


Individual carbon chains show high resilience, but long time stability it is currently not known
Scaling of Carbon Memory: porous carbon

- very high variability is expected once the structure size scales down to the size of the constituents (CNTs, voids etc.) example CNT ribbon:

- depending on the location of the top electrode (blue), there will be a void or a lot of CNTs \( \Rightarrow \) high variability
- more accurate assembly is required (aligned SWCNTs) to make variability smaller
Scaling of Carbon Memory: Contact Resistance

- Biggest threat for scaling (ReRAM) might come from contact resistance.
- Scales with area – what worked at ~100 nm, doesn't at ~10 nm!
- Associated voltage drop at high current densities is very high.

<table>
<thead>
<tr>
<th>J</th>
<th>CR 1E-6</th>
<th>CR 1E-7</th>
<th>CR 5E-8</th>
</tr>
</thead>
<tbody>
<tr>
<td>10 MA/cm²</td>
<td>10 V</td>
<td>1 V</td>
<td>0.5 V</td>
</tr>
<tr>
<td>1 MA/cm²</td>
<td>1 V</td>
<td>0.1 V</td>
<td>0.05 V</td>
</tr>
</tbody>
</table>
In advanced nodes the interconnect wiring plays an active element due to IR-drop and RC-delay in wires & contacts. Operating with fast pulses will be challenging or impossible. A possible solution would be to operate the memory array in the capacitance discharge mode:

The interconnect wires are precharged to V by the x-access point while the y-access is still floating. After precharging, the x-access is disconnected. The energy \( \frac{1}{2} CV^2 \) that is stored in the interconnects is discharged to ground or even negative voltage by enabling the y-access. This approach guarantees that the wiring is discharged after the pulse and no set after reset can happen.
Current State-Of-The Art For Carbon Memory Technology


- Only single cells
- This work has high capacitance layout
- Real time-resolved switching currents are not measured, but for set, at least an external current limiting resistor has been used
- Good data retention at 300° C for 600 min
Current State-Of-The Art For Carbon Memory Technology


- Only single cells, 18 nm thick a-C:H film
- High capacitance layout
- Demonstrates **what is needed**: time-resolved current to be measured starting from the first forming event to reset & set
- On-chip resistor has been used to **limit current overshoot**
Current State-Of-The Art For Carbon Memory Technology

The most advanced studies with results from 4 Mb arrays are based on porous CNT-ribbon memory from the company Nantero (References [44, 45, 46, 47, 48])

- 4Mb arrays in 0.25 μm CMOS, some 20 nm cells are reported
- First pulse requirements are not reported and might be high
- $10^{11}$ endurance cycles on some cells with high capacitance layout are reported with 20 ns pulses (VLSI 2014)
- Switching currents vary and are estimated from gate voltage on huge transistor biased close to $V_{th}$ (which have big variations) or are measured on individual cells to be in the order of 20-30 μA
- Overall, the published data are somewhat inconsistent

Challenge of Predicting Technology Performance

- Real Chip layout and technology are needed
- But these are proprietary data, which are not disclosed
- Example: well-known DRAM chips run same task, same JEDEC specs, different vendors and technologies

- Even idle currents are 3x different!
## Appendix 1: Metrics for memory device assessment

<table>
<thead>
<tr>
<th>Description</th>
<th>Unobtainable-RAM (e.g., “Ideally…”)</th>
<th>CARBON MEMORY</th>
<th>Comments (including any associated tradeoffs)</th>
</tr>
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<tbody>
<tr>
<td><strong>Scalability</strong></td>
<td>Each layer @ 4F^2 down to beyond 12nm node</td>
<td>@ 4F^2 down to single atomic bonds</td>
<td>both memory cell AND wire pitch can be scaled. But care needs to be taken about the select device. Major threat comes from contact resistances</td>
</tr>
<tr>
<td><strong>Multi-level cells (MLC)</strong></td>
<td>Up to 3bits/cell</td>
<td>2 bits/cell are demonstrated [48], Recommended is 1bits/cell</td>
<td>MLC in RRAM is possible for relaxed feature sizes. IF RC from interconnects play an important role only, Ron &gt; 200 kOhm might be accessible</td>
</tr>
<tr>
<td><strong>Multi-layer stacking</strong></td>
<td>At least 32 layers</td>
<td>8-12 Multilayer might be possible</td>
<td>BEOL compatibility depends on the select device. Complicated stacks needs to be etched at 8-12 layer. 3D monolithic integration might be feasible</td>
</tr>
<tr>
<td><strong>Fabrication costs</strong></td>
<td>Total cost very similar to current NAND or lower</td>
<td>Similar to PCM or RRAM</td>
<td>Number of critical mask steps= 1 for 1layer CMOS - No new/difficult unit processes - New/difficult materials only with nanotubes, a-C is known to be compatible with CMOS processing- device forming is necessary (first pulse challenge)!</td>
</tr>
</tbody>
</table>
| **Array efficiency**         | >100% (circuitry tucked underneath, w/ extra Si real-estate left over) | Similar to PCM or RRAM | • BL/WL lengths  
• Extent of peripheral circuitry  
• Peripheral circuitry play a critical role (such as compliance, or current limiting needed for low power  
• Interplay with 3D stacking |
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<td><strong>State-of-the-art</strong></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Array size</td>
<td>N/A (Unobtainable-RAM has not been demonstrated)</td>
<td>4 Mbit [45]</td>
<td>obtained individually...</td>
</tr>
<tr>
<td>Yield</td>
<td>N/A</td>
<td>Not known</td>
<td></td>
</tr>
<tr>
<td>Technology node</td>
<td>N/A</td>
<td>20 nm cells demonstrated (in public domain) [45]</td>
<td>But not for both the implemented CMOS device AND for the wiring pitch (CMOS 0.25 µm) First current pulse issue not investigated</td>
</tr>
<tr>
<td><strong>Latency</strong></td>
<td></td>
<td></td>
<td></td>
</tr>
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</table>
| Read latency              | < 10ns (for memory applications)     | ~50 ns for 1 [45] ~30 ns for 0 [45] | • read contrast ~1000  
                           | (~1us for storage applications)     |                                           | • Size of read window  
                           |                                      |                                           | • Read disturb issues  
                           |                                      |                                           | • Errors from crosstalk  
                           |                                      |                                           | = all depend on chip design |
| Write latency             | < 20ns (for memory applications)     | ~20 ns [48]   | • Requires verify-after-write/erase  
                           | (~1us for storage applications)     |                                           | • Write disturb of other devices = research  
                           |                                      |                                           | • Damage threshold to avoid? = research  
                           |                                      |                                           | • write-in-place supported  
                           |                                      |                                           | = all depend on chip design    |
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<td><strong>Power / Energy</strong></td>
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<td></td>
<td></td>
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<tr>
<td>Read power / Energy</td>
<td>&lt; 1/10 scaled DRAM for memory applications (for storage applications, same as scaled NAND or better)</td>
<td>1V/10 nA  1V/10µA</td>
<td>Power $\rightarrow$ parallelism $\rightarrow$ bandwidth Roadmap with scaling Please specify power usage... • ...by selected devices • ...elsewhere in the array (leakage, line resistances), and • ...in peripheral circuitry = depends on proprietary chip design...</td>
</tr>
<tr>
<td>Write power / Energy</td>
<td>for memory applications, &lt; 1/5 scaled DRAM (for storage applications, &lt;5x read power)</td>
<td>15pJ/bit [48]</td>
<td>Power $\rightarrow$ parallelism $\rightarrow$ bandwidth Roadmap with scaling? power usage... • ...by selected devices • ...elsewhere in the array (leakage, line resistances), and • ...in peripheral circuitry = depends on proprietary chip design...</td>
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<td><strong>Reliability</strong></td>
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| Endurance | >>1e12 (memory applications)  
(>1e9, storage applications) | >1e11 [48] | • Can device failures be predicted  
= research subject, scales with node...  
• Devices fail to what state?  
= research subject, scales with node...  
• Do failed devices affect neighbors?  
= research subject, depends on design  
• Impact on other characteristics? (e.g., do cycled devices behave differently?)  
= research subject, scales with node...  
• Are failures random or clustered?  
= research subject, scales with node... |
| Retention | >1 month @ 85°C (memory)  
>10 years @ 150°C (storage) | >10 years @ 120°C  
300 min @ 300 C [41]  
168 h @ 250 C [44] | tradeoffs, between retention & write-speed, or retention & cycling?  
= research subject, scales with node... |
| Variability | Extremely low (e.g., 6th-sigma device also meets all specs) | If we would have 6 sigma, we would have a product... | Intra-device & inter-device – variability & repeatability?  
= research subject, scales with node...  
Porous carbon will have a problem at small dimension |
Selected Literature


Selected Literature

Selected Literature


Electrode Diffusion: A Consequence of High Current Density