

Nanomagnetic Logic

A path towards 3D monolithic integration

Habilitationsschrift

Wissenschaftliche Arbeit zur Erlangung des Grades
Dr.-Ing. habil.
an der Fakultät für Elektrotechnik- und Informationstechnik
der Technischen Universität München.

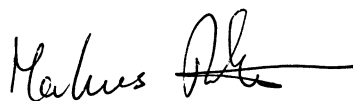
Dr.-Ing. Markus Becherer
Lehrstuhl für Nanoelektronik

Vorsitz des Fachmentorats: Prof. Franz Kreupl

1. Fachmentor: Prof. Paolo Lugli

2. Fachmentor: Prof. Wolfgang Porod, University of Notre Dame, USA.

Vorgelegt im November 2016.



München, 11.11.2016, Markus Becherer

Contents

| | | |
|-----|--|-----|
| I | Nanomagnetic Logic Research at TUM: An Overview | 5 |
| 1 | Beyond CMOS | 7 |
| 1.1 | Logic with inherent memory | 9 |
| 1.2 | Field-Coupled computing in stacks of magnetic bilayers | 9 |
| 1.3 | The pNML operation principles | 12 |
| 1.4 | Major building blocks of planar 2D pNML | 14 |
| 1.5 | Adopting the 5 tenets for digital computation with pNML | 16 |
| 2 | The vision of monolithic 3D integration with pNML | 18 |
| 2.1 | A proof-of-principle experiment for 3D stacked NML | 19 |
| 2.2 | Basic technology for 3D NML fabrication | 20 |
| 2.3 | Major building blocks of 3D pNML | 22 |
| 3 | A 3D pNML BEOL co-processing unit | 24 |
| 3.1 | Electrical I/O | 25 |
| 3.2 | Conservative metrics: cost, size, speed | 26 |
| 3.3 | Progressive characteristics of NML | 27 |
| 3.4 | Summary | 28 |
| II | Monolithic 3D Integration of pNML: Author's Publications | 35 |
| 4 | Nonreciprocal information transport in field-coupled Co/Pt islands | 39 |
| 5 | Basic electrical I/O devices | 53 |
| 6 | A non-volatile logic family – 2D pNML | 69 |
| 7 | On-chip clocking as power supply | 97 |
| 8 | Monolithic 3D integration of pNML | 111 |
| 9 | The vision of a 3D-integrated nanomagnetic CPU | 129 |